

**Department of Physics**

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| Course Number | COE 328 |
| Course Title | Digital Circuits |
| Semester/Year | Fall 2021 |
| Instructor | Dr. Reza Sedaghat |
| TA Name | Sajjad Rostami Sani |

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| Lab/Tutorial Report No. | 4 |
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| Report Title | Lab 4 |

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| Section No. | 03 |
| Submission Date | 15-11-2021 |
| Due Date | 15-11-2021 |

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**Objective**

The objective of this lab was to build a 4:1 multiplexer circuit using 3 2:1 multiplexer circuit and to build a 3:8 decoder circuit using 2 2:4 decoders.

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**Procedure**

Part 1:

VHDL code for 2:1 multiplexer

Text

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VHDL code for 4:1

Text

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Circuit of 4:1 multiplexer using 3 2:1 multiplexers

Diagram

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Diagram

Description automatically generated

Waveform of 1:4 multiplexer circuit

A picture containing diagram

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Part 2:

VHDL code for 2:4 decoder

Text

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Circuit of 3:8 decoder using 2 2:4 decoders a NOT gate and 2 AND gates

Diagram, schematic

Description automatically generated

Diagram, schematic

Description automatically generated

Waveform of 3:8 decoder circuit

Graphical user interface

Description automatically generated with medium confidence

**References**

Brown, S. D., & Vranesic, Z. G. (2009). *Fundamentals of Digital Logic with VHDL Design*. New York, United States: McGraw-Hill Education.